

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re Application of:**

Nishant Sinha

**Serial No.:** 10/668,914

**Filed:** September 23, 2003

**For:** PROCESS AND INTEGRATION  
SCHEME FOR FABRICATING  
CONDUCTIVE COMPONENTS,  
THROUGH-VIAS AND  
SEMICONDUCTOR COMPONENTS  
INCLUDING CONDUCTIVE THROUGH-  
WAFER VIAS

**Confirmation No.:** 2525

**Examiner:** W. Lindsay Jr.

**Group Art Unit:** 2812

**Attorney Docket No.:** 2269-5859US  
(02-0390.00/US)

**Notice of Allowance Mailed:**

March 22, 2007

**VIA ELECTRONIC FILING  
JUNE 20, 2007**

**FEE ADDRESSEE FOR RECEIPT OF PTO NOTICES  
RELATING TO MAINTENANCE FEES**

Mail Stop ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

1. This letter is to specify that the FEE ADDRESSEE for this patent is:

Serial No.: 10/668,914

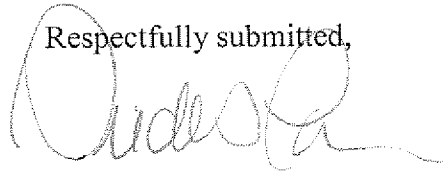
MICRON TECHNOLOGY, INC.

Mail Stop 525  
8000 South Federal Way  
Boise, Idaho 83707-0006

2. The Customer Number for the Fee Addressee is **26809**.
3. Any prior FEE ADDRESSEE for this patent is hereby revoked.
4. It is certified that the person whose signature appears below has the authority to

change the FEE ADDRESSEE for this patent.

Respectfully submitted,



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Date: June 20, 2007

BGP/ps:eg

Document in ProLaw